

## A Vision for IC DFM

Many EDA startups got funded in the last 3 years to address Design For Manufacturability of Chips. Catena, however, was an internal Cadence project that finally sees light of day.

Catena does post-layout optimization on shape-based parameters (vias, wires) to arrive at a better interconnect design, before handing off to the Fab or the Foundry.

As chips gets denser and denser, the pressure on layout engines intensifies, to accomodate all this functionality within a tiny perimeter. The victim, naturally, is yield.

Hence, the chip industry has been looking for ways to handle yield issues at the design stage.

This step is one in the right direction.

However, it is still a long way from being able to do predictive modeling using parameters of the manufacturing process before and during layout. Setting constraints and catching violations or risks pre- and during layout are still more valuable than correcting things after, as the degrees of freedom tend to go down dramatically as the process progresses.

Catena, therefore, is only a tiny step in the direction of a massive and ambitious vision that many in the industry harbor. My articulation of this vision is as follows: An exhaustive Design Rule Checker (DRC) that contains in its heart an Expert System that understands the manufacturing Process and Equipments, Properties of Materials, Temperatures, Signal Integrity, Power and Voltage issues, etc. This uber-DRC will then run through its rule-base - every Layout decision, make estimates about downstream Layout options/decisions (like a Chess Player), and help along the Layout optimization process.

And a lot more!

Source: <http://www.articlecircle.com>

### About the Author

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